AMENDMENTS TO THE CLAIMS

1. (Cancelled)

2. (Previously Presented) The integrated circuit system as in claim 10, wherein each of the plurality of internal voltage supply generators regulate the internal voltage supply generated there from.

3. (Previously Presented) The integrated circuit system as in claim 10, wherein the external voltage is greater than the internal voltage supply.

4. (Previously Presented) The integrated circuit system as in claim 10, further comprising a scan-chain formed by a chain of scannable register latches storing fuse information and a switch enable/disable signal.

5–7. (Cancelled)

8. (Previously Presented) The integrated circuit system as in claim 10, wherein a feedback voltage is provided from the charge pump to the voltage limiter.

9. (Previously Presented) The integrated circuit system as in claim 10, wherein the external voltage drives the reference supply unit, the voltage limiter, the oscillator, and the charge pump.

10. (Currently Amended) An integrated circuit system having a plurality of macros, said integrated circuit system comprising:

an external voltage supply input configured for supplying an external voltage to the integrated circuit; and

a plurality of internal voltage supply generators, each connected to a respective macro of the plurality of macros and configured for receiving the external voltage, generating an internal

voltage supply, and using said generated internal voltage supply for operating its respective macro, wherein each of the plurality of internal voltage supply generators includes

a reference supply unit for generating at least one of a voltage level and a current level,

a voltage limiter coupled to the reference supply unit for controlling a voltage output level outputted from the voltage limiter,

an oscillator coupled to the voltage limiter for receiving the voltage output level and generating an oscillating voltage level,

a charge pump for receiving the oscillating voltage level for generating the internal voltage supply,

a reference voltage generator for generating and providing a reference voltage for driving at least one voltage generator, wherein the reference voltage generator and the at least one voltage generator provide voltage to a substrate bias level voltage generator, a negative word line level voltage generator, and a boosted wordline high level voltage generator, and

an enable register coupled to the voltage limiter, the oscillator and the charge pump, wherein the enable register is configured for storing one of an enable and disable signal, for isolating each of the plurality of macros from the external voltage supply, and for enabling or disabling at least the voltage limiter, the oscillator and the charge pump according to the stored signal.

11. (Original) The integrated circuit system as in claim 10, wherein the enable register stores one of an enable and a disable signal during a power-on period.

12. (Cancelled)

13. (Previously Presented) The integrated circuit system as in claim 20, further comprising a scan-chain formed by a chain of scannable register latches storing fuse information and the enable/disable signal.

14. (Previously Presented) The integrated circuit system as in claim 20, wherein the second means comprise a reference voltage generator for generating and providing a reference

voltage for driving at least one voltage generator.

15. (Original) The integrated circuit system as in claim 14, wherein the reference voltage generator and the at least one voltage generator provide voltage to the at least one of the plurality of internal voltage supply generators.

16–17. (Cancelled)

18. (Previously Presented) The integrated circuit system as in claim 20, wherein a feedback voltage is provided from the charge pump to the voltage limiter.

19. (Previously Presented) The integrated circuit system as in claim 20, wherein the external voltage drives the reference supply unit, the voltage limiter, the oscillator, and the charge pump.

20. (Currently Amended) An integrated circuit system having a plurality of macros, said integrated circuit system comprising:

first means for receiving an external voltage; and

second means for generating an internal voltage supply and using said generated internal voltage supply for operating at least one of a plurality of internal voltage supply generators coupled to a respective macro of the plurality of macros, the at least one of the plurality of internal voltage supply generators is selected from the group consisting of a substrate bias level voltage generator, a negative word line level voltage generator, and a boosted wordline high level voltage generator, the second means being coupled to the first means, wherein the second means includes:

a reference supply unit for generating at least one of a voltage level and current level,

a voltage limiter coupled to the reference supply unit for controlling a voltage output level outputted from the voltage limiter,

an oscillator coupled to the voltage limiter for receiving the voltage output level and generating an oscillating voltage level,

a charge pump for receiving the oscillating voltage level for generating the internal

voltage supply, and

at least one enable register coupled to the voltage limiter, the oscillator and the charge pump, wherein the at least one enable register is configured for storing an enable/disable signal, for isolating each of the plurality of macros from the external voltage, and for enabling or disabling at least the voltage limiter, the oscillator and the charge pump according to the stored enable/disable signal.

21. (Previously Presented) The integrated circuit system as in claim 20, wherein at least one enable register stores the enable/disable signal during a power-on period.

22. (Original) The integrated circuit system as in claim 20, further comprising means for performing a built-in self test for testing the DC voltage generator system.